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High-Performance ALU Architecture Using MGDI Based Logic Gates and Multiplexers

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Abstract: This project presents the design of a low-power and area-efficient Arithmetic Logic Unit (ALU) using the Modified Gate Diffusion Input (MGDI) and Hybrid GDI design techniques. Unlike conventional GDI-based architectures, the proposed design implements all fundamental logic gates, including AND, OR, XOR, NAND, NOR, NOT, and a 2:1 multiplexer using Hybrid GDI logic to achieve improved performance and full voltage swing. These optimized building blocks are utilized to construct the full adder, full subtractor, decoder, and the complete ALU architecture. The proposed implementation significantly reduces transistor count, switching activity, propagation delay, power consumption, and silicon area compared to conventional CMOS and standard GDI implementations. The circuits are designed and verified using Tanner EDA at the 250 nm CMOS technology node and extended to 60nm. Simulation results demonstrate that the proposed Hybrid GDI ALU offers superior energy efficiency while maintaining reliable logic operation, making it suitable for modern low-power VLSI systems and portable electronic applications.

Introduction: While lowering the no of transistors and decreasing the frequency of switching activities are prevalent techniques of reducing power consumption and area in ALU. First, while supply voltage reduction effectively lowers power consumption, its application is limited to the functional units in the ALU circuits. The project proposes a design for low power area optimized consumption ALU that exploits the benefits of offline software, which can work alone in delivering minimum power consumption or work alongside supply voltage reduction technology to deliver even lower power consumption. Our ALU architecture consists of a set of fast and slow functional units. There are many advantages and plus points to the design of our ALU. Not only does it consume minimal power during runtime, it does not require real time process to monitor performance. Neither is a hardware circuit needed to tune the supply voltage. Compared with other models operating on the supply voltage reduction principle, the ALU we have designed is far simpler. Low power and High speed are the design trade-offs in VLSI industry. Power consumption, area, speed, noise immunity has emerged as a primary design constraints for integrated circuits (ICs). The VLSI designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. Most of the Very Large Scale IC (VLSI) applications, Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire

computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. In this paper, from different existed base papers several full adder circuits based on different low power techniques have been proposed targeting Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. In the era of growing technology and scaling of devices up to nanometer regime, the arithmetic logic circuits are to be designed with compact size, less power and propagation delay. Arithmetic operations are indispensable and basic functions for any high speed low power application digital signal processing, microprocessors, image processing etc.Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell. There are various topologies and Methodologies proposed to design full adder cell efficiently. WHIS rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts [1]–[3]. The wish to improve the performance of logic circuits, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last two decades [17]. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Formal methods for deriving pass-transistor logic have been presented for nMOS. They are based on the model, where a set of control signals is applied to the gates of nMOS transistors. Another set of data signals are applied to the sources of the n-transistors [1].

LITERATURE SURVEY: There are different types and designs of full adder which is discussed in various papers at state of the art level andprocess and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS,C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f. R. Shalem, E. John, and L.K. John, proposed a conventionalCMOS full adder consisting of 28 transistors [1]. Later, the number of transistor count is reduced to have less area andpower consumption. A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used [2]. The Complementary Passtransistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw [3]. A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The powerconsumption of this structure is 12µw. N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62µw. Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23µw [3]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistorusing Dual Threshold Node Design with Submicron Channel Length [4]. T. Vigneswaran, B. Mukundhan, and P.Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to50% [5]. Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area.T. Esther Rani, M. Asha Rani, Dr.RameshwarRao, designed an

area optimized low power arithmetic and logic unit inwhich Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [6].Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm UsingGDI Technique and Its Performance Comparison [7].

PROPOSED METHOD:

MODIFIED GATE DIFFUSION TECHNIQUE (M-GDI): Modified Gate Diffusion Technique (M-GDI) is another technique to design Digital circuits in order to get better performance compared to CMOS and PTL (Pass Transistor Logic). It minimizes the required number of transistor resulting decrease in area of the circuit, power dissipation and

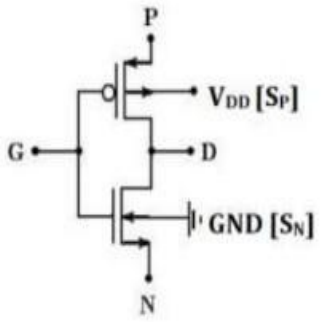

Fig1 Bais MGDI

delay for better implementation. M-GDI technique is very close to GDI technique as it can be achieved by connecting the bulk nMOS to GND (Ground – 0 V) and bulk pMOS to VDD (Power Supply) to overcome the difficulties of fabricating which occurs in standard CMOS process. It can also be implemented by twin cell CMOS technique and Silicon on Insulator (SoI) technique.

3-T XOR using m-GDI Technique: The input (A) is fed to the source terminal of pMOS as well as the gain terminal of pMOS, the second input (B) is fed to the common gate input terminal of both pMOS and nMOS as well as to the source terminal of the pMOS in order to implement the XOR the source terminal is grounded hence the desired output is obtained from the common drain terminal of the three transistors.

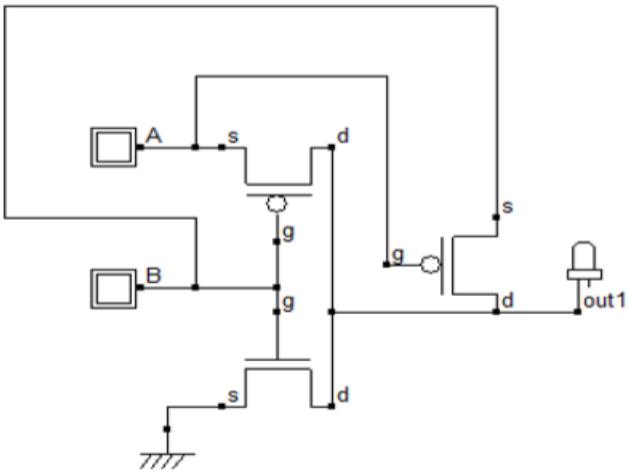

Figure:2 3-T XOR Transistor Level Design

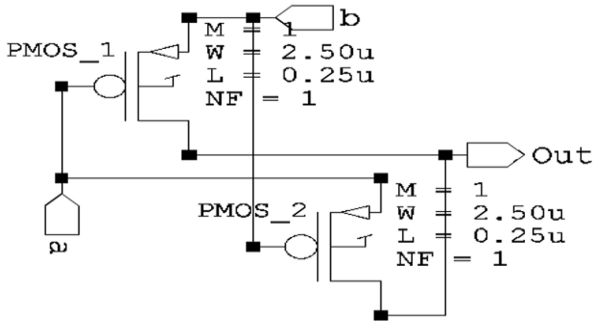

Fig:3 2T Xor Gate

2-T 2:1 MUX using GDI Technique

The input (A) is fed to the source of the pMOS, the input

• (B) is fed to the drain terminal of the nMOS, and the select line input is fed to the common gate input to both of the transistors (nMOS and pMOS) as the 2:1 MUX is realized by gaining output from the output terminal.

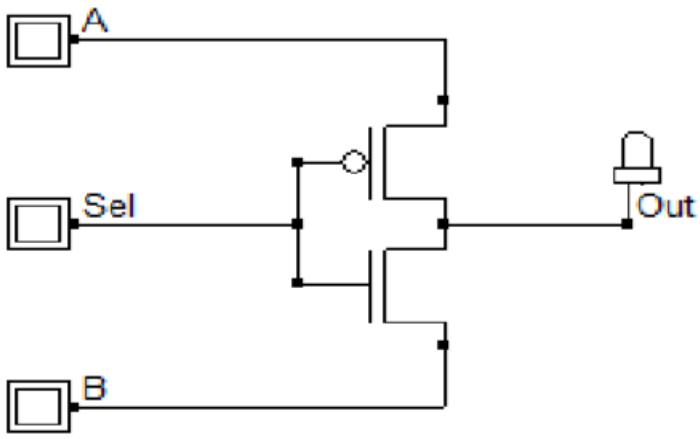

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Fig4. 2-T OR using GDI Technique

• The input (A) is fed through the common gate input terminal of both the transistors (nMOS and pMOS) input (B) is fed through the source of pMOS as we have constructed a two input OR gate the drain terminal of nMOS is fed with a constant positive supply.

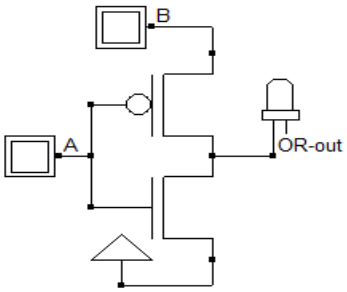

Figure5 2-T OR Transistor Level design

2-T AND USING MGDI TECHNIQUE : The input (A) is fed to the common gate input terminal of both of the transistors (nMOS and pMOS), input (B) is fed to the drain terminal of nMOS as two input AND gate is constructed the input to the source of pMOS is grounded.

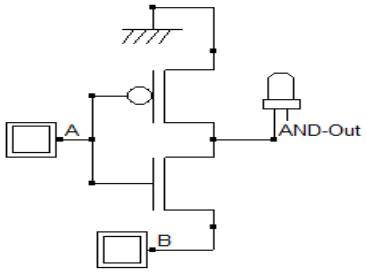

Figure 6:2-T AND Transistor Level Design

DECODER: A decoder is a combinational logic circuit that is used to change the code into a set of signals. It is the reverse process of an encoder. A decoder circuit takes multiple inputs and gives multiple outputs. A decoder circuit takes binary data of 'n' inputs into '2^n' unique output. In addition to input pins, the decoder has a enable pin.

3 to 8 DECODERS (Stand alone).

Eight outputs (DO to D7) and three inputs (A, B, and C) make up a 3 to 8 decoder.A single output out of the eight is chosen based on the three inputs. The table below displays the truth table for three to eight decoders.

A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table: The truth table of 3: 8 decoder is shown below.

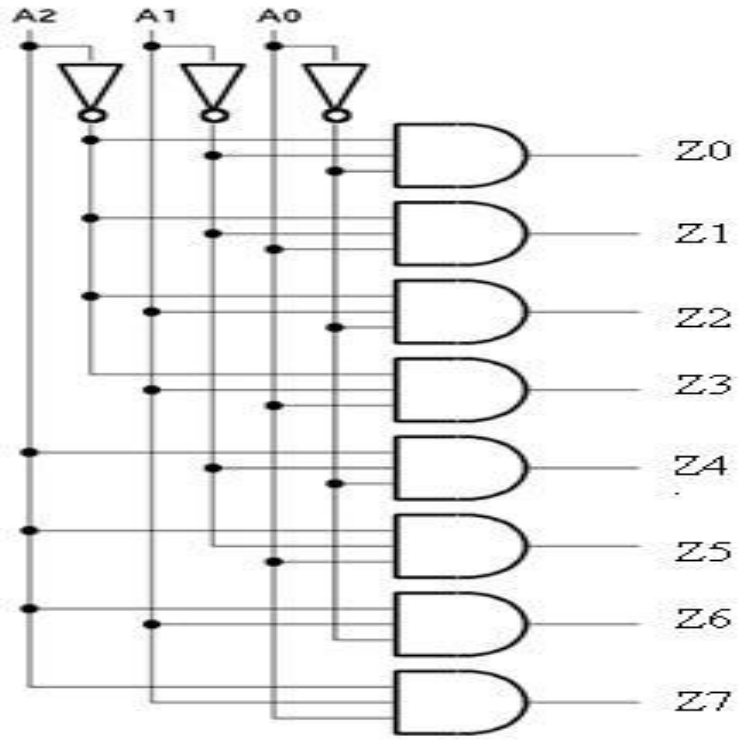

Fig:7 3-8 Decoder digital diagram

And gate and not gate in above diagram are designed using MGDI basic gates as shown in above section.

RESULTS:

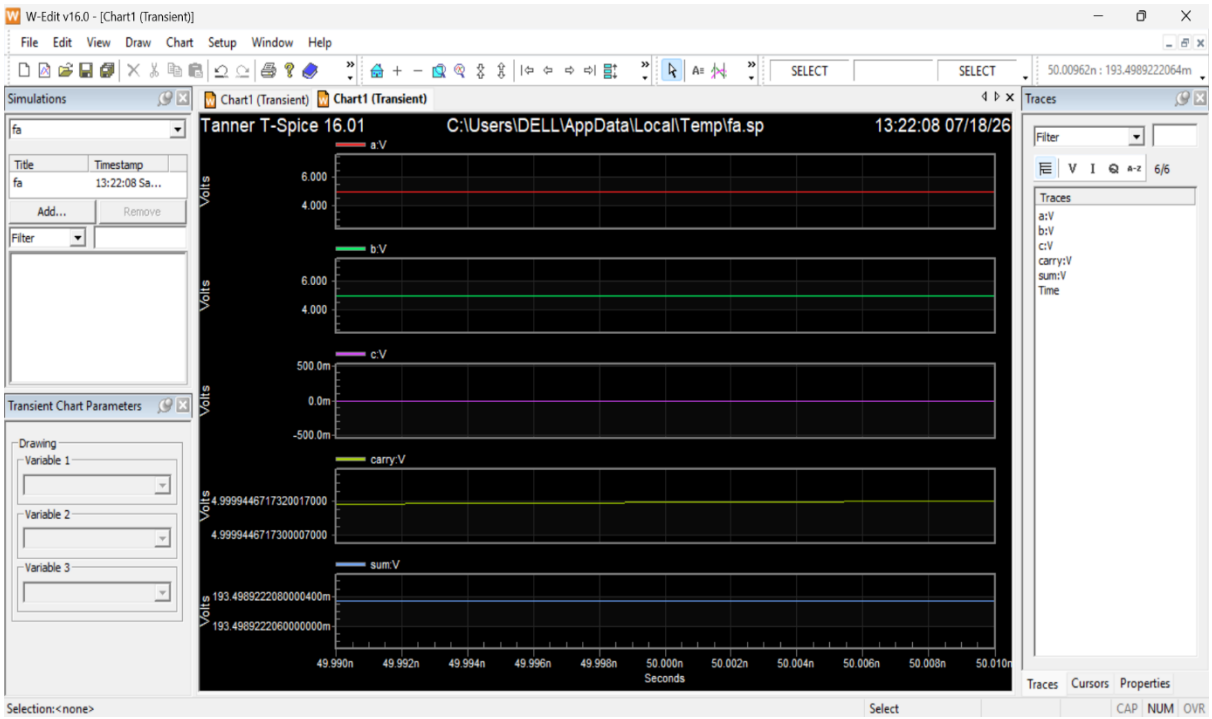

Fig a: Simulation result1

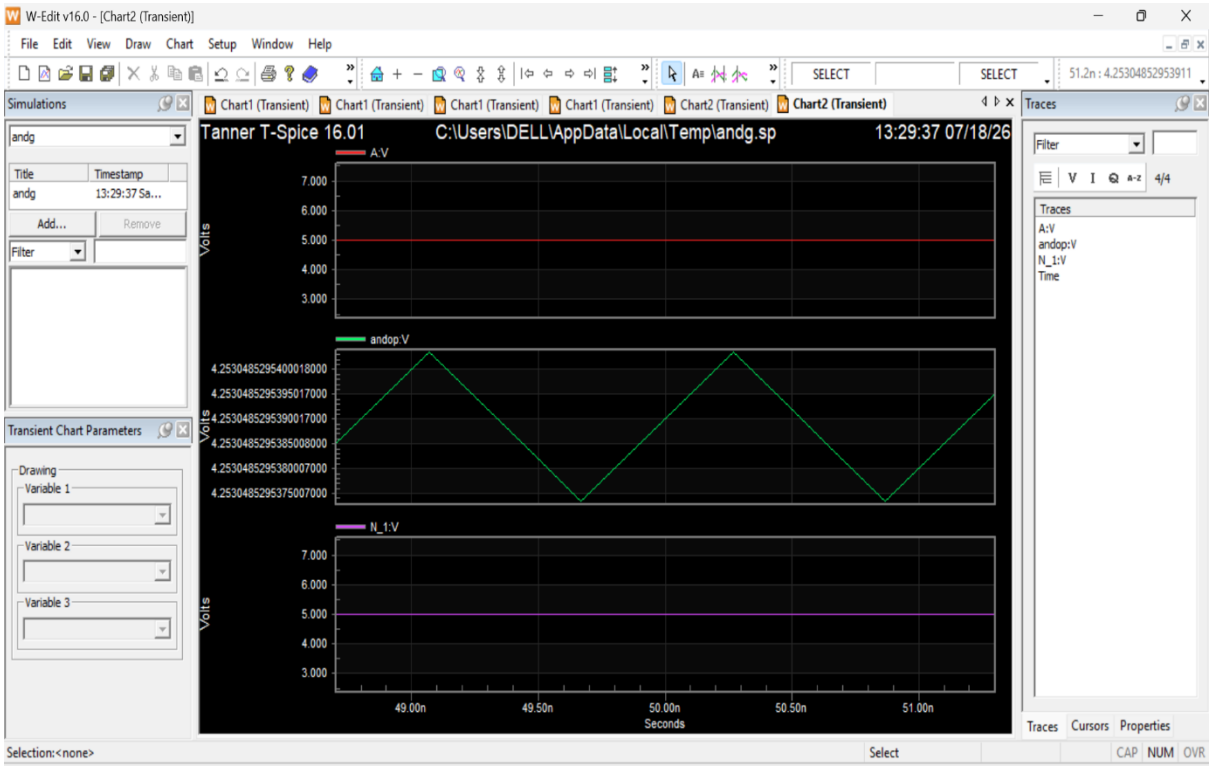

Fig b: Simulation result2

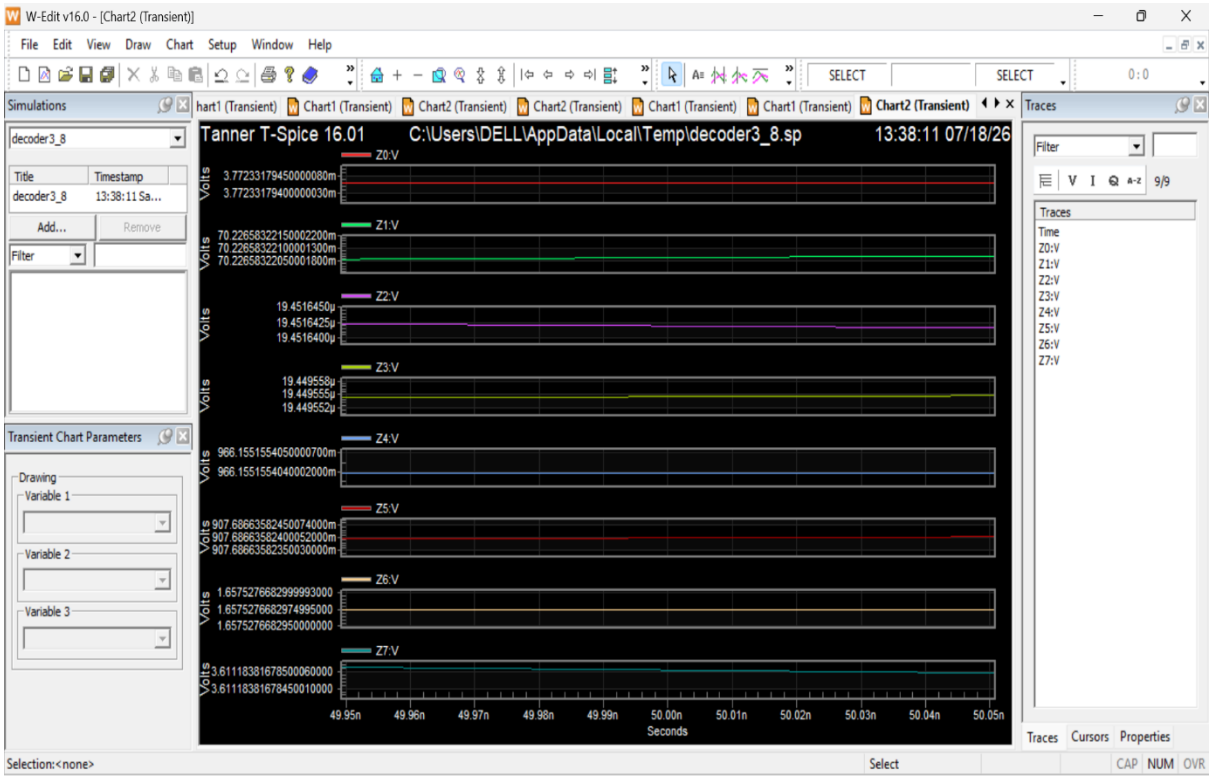

Fig c: Simulation result3

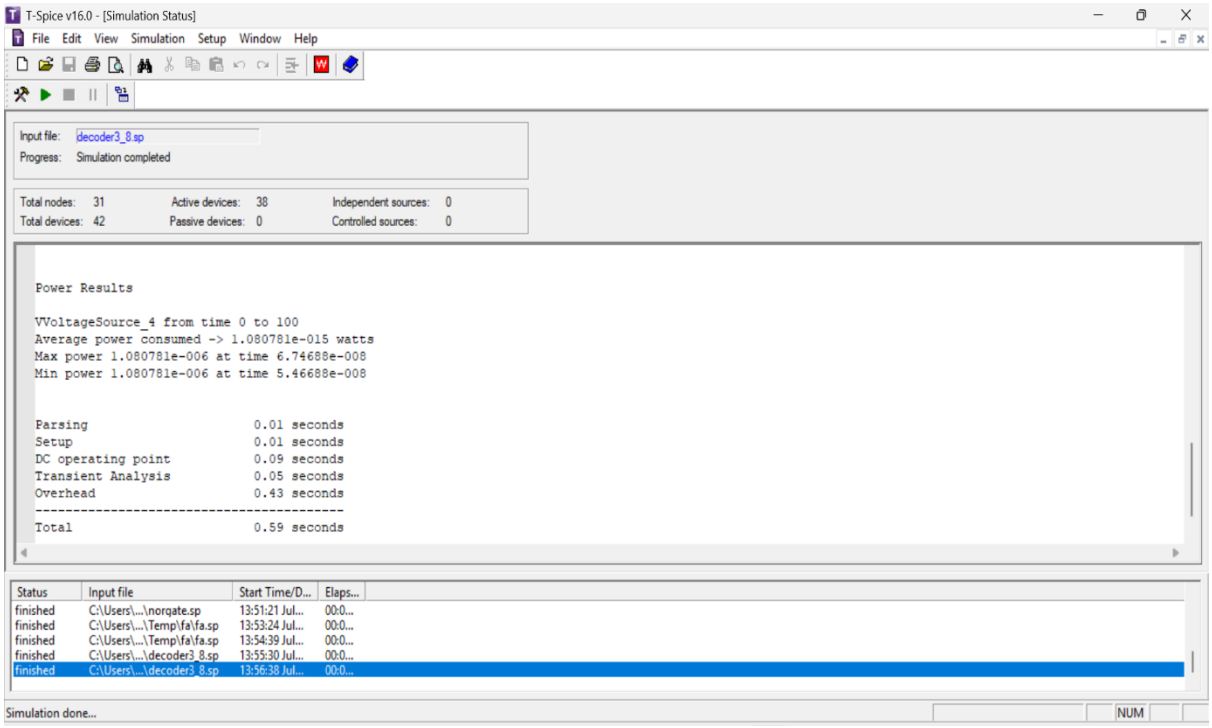

Fig e: synthesis result1

CONCLUSION: The proposed ALU based on Modified GDI and Hybrid GDI techniques successfully improves the overall performance of arithmetic and logic circuits by optimizing every fundamental building block rather than only the XOR gate. All basic logic gates, along with the 2:1 multiplexer, full adder, full subtractor, and decoder, were implemented using Hybrid GDI logic, resulting in a compact and efficient architecture. The reduction in transistor count directly contributes to lower power dissipation, smaller silicon area, and reduced propagation delay. Simulation results obtained using Tanner EDA validate that the proposed design performs better than conventional CMOS and standard GDI implementations in terms of power, area, and speed. Therefore, the proposed Hybrid GDI ALU provides an effective solution for designing energy-efficient arithmetic units in modern VLSI systems.

FUTURE SCOPE The proposed work can be extended in several directions to further enhance performance and applicability:

- Design higher-bit ALUs (16-bit, 32-bit, and 64-bit) using the Hybrid GDI approach.
- Implement multiplication and division units using Hybrid GDI logic.
- Evaluate performance in advanced CMOS technologies such as 90 nm, 65 nm, 45 nm, 28 nm, and FinFET technologies.
- Optimize the design for ultra-low-voltage and near-threshold operation.
- Perform physical layout implementation and post-layout verification.
- Incorporate pipelining for high-speed processor architectures.

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